WEST

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Search Results -

Terms	Documents
(bus$3 or (sub adj1 bus$3)) same (bundl$3 or group$1 or together or package$1) same ((data adj1 flow adj1 processor$1) or (programmable adj1 gate adj1 array$1))	61

Database: US Patents Full-Text Database
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IBM Technical Disclosure Bulletins

Refine Search: (bus$3 or (sub adj1 bus$3)) same (bundl$3 or group$1 or together or package$1) same ((data adj1 flow adj1

Clear

Search History

Today's Date: 4/20/2001

DB Name	Query	Hit Count	Set Name
USPT	(bus$3 or (sub adj1 bus$3)) same (bundl$3 or group$1 or together or package$1) same ((data adj1 flow adj1 processor$1) or (programmable adj1 gate adj1 array$1))	61	L1

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Search Results -

Terms	Documents
(bus$3 or (sub adj1 bus$3)) same (bundl$3 or group$1 or together or package$1) same ((data adj1 flow adj1 processor$1) or (gate adj1 array$1))	226

Database: US Patents Full-Text Database
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Refine Search: (bus$3 or (sub adj1 bus$3)) same (bundl$3 or group$1 or together or package$1) same ((data adj1 flow adj1

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Search History

Today's Date: 4/20/2001

DB Name	Query	Hit Count	Set Name
USPT	(bus$3 or (sub adj1 bus$3)) same (bundl$3 or group$1 or together or package$1) same ((data adj1 flow adj1 processor$1) or (gate adj1 array$1))	226	L2
USPT	(bus$3 or (sub adj1 bus$3)) same (bundl$3 or group$1 or together or package$1) same ((data adj1 flow adj1 processor$1) or (programmable adj1 gate adj1 array$1))	61	L1

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Search Results -

Terms	Documents
(bus$3 or (sub adj1 bus$3)) same (bundl$3 or group$1 or together or package$1) same ((data adj1 flow adj1 processor$1) or (gate adj1 array$1))	8

Database:
- US Patents Full-Text Database
- US Pre-Grant Publication Full-Text Database
- JPO Abstracts Database
- EPO Abstracts Database
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- IBM Technical Disclosure Bulletins

Refine Search: (bus$3 or (sub adj1 bus$3)) same (bundl$3 or group$1 or together or package$1) same ((data adj1 flow adj1 Clear

Search History

Today's Date: 4/20/2001

DB Name	Query	Hit Count	Set Name
JPAB	(bus$3 or (sub adj1 bus$3)) same (bundl$3 or group$1 or together or package$1) same ((data adj1 flow adj1 processor$1) or (gate adj1 array$1))	8	L3
USPT	(bus$3 or (sub adj1 bus$3)) same (bundl$3 or group$1 or together or package$1) same ((data adj1 flow adj1 processor$1) or (gate adj1 array$1))	226	L2
USPT	(bus$3 or (sub adj1 bus$3)) same (bundl$3 or group$1 or together or package$1) same ((data adj1 flow adj1 processor$1) or (programmable adj1 gate adj1 array$1))	61	L1

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Search Results -

Terms	Documents
(bus$3 or (sub adj1 bus$3)) same (bundl$3 or group$1 or together or package$1) same ((data adj1 flow adj1 processor$1) or (gate adj1 array$1))	10

Database: US Patents Full-Text Database; US Pre-Grant Publication Full-Text Database; JPO Abstracts Database; EPO Abstracts Database; Derwent World Patents Index; IBM Technical Disclosure Bulletins

Refine Search: (bus$3 or (sub adj1 bus$3)) same (bundl$3 or group$1 or together or package$1) same ((data adj1 flow adj1 Clear

Search History

Today's Date: 4/20/2001

DB Name	Query	Hit Count	Set Name
EPAB	(bus$3 or (sub adj1 bus$3)) same (bundl$3 or group$1 or together or package$1) same ((data adj1 flow adj1 processor$1) or (gate adj1 array$1))	10	L4
JPAB	(bus$3 or (sub adj1 bus$3)) same (bundl$3 or group$1 or together or package$1) same ((data adj1 flow adj1 processor$1) or (gate adj1 array$1))	8	L3
USPT	(bus$3 or (sub adj1 bus$3)) same (bundl$3 or group$1 or together or package$1) same ((data adj1 flow adj1 processor$1) or (gate adj1 array$1))	226	L2
USPT	(bus$3 or (sub adj1 bus$3)) same (bundl$3 or group$1 or together or package$1) same ((data adj1 flow adj1 processor$1) or (programmable adj1 gate adj1 array$1))	61	L1

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Search Results -

Terms	Documents
(bus$3 or (sub adj1 bus$3)) same (bundl$3 or group$1 or together or package$1) same ((data adj1 flow adj1 processor$1) or (gate adj1 array$1))	8

Database:
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- US Pre-Grant Publication Full-Text Database
- JPO Abstracts Database
- EPO Abstracts Database
- Derwent World Patents Index
- IBM Technical Disclosure Bulletins

Refine Search: (bus$3 or (sub adj1 bus$3)) same (bundl$3 or group$1 or together or package$1) same ((data adj1 flow adj1 Clear

Search History

Today's Date: 4/20/2001

DB Name	Query	Hit Count	Set Name
DWPI	(bus$3 or (sub adj1 bus$3)) same (bundl$3 or group$1 or together or package$1) same ((data adj1 flow adj1 processor$1) or (gate adj1 array$1))	8	L5
EPAB	(bus$3 or (sub adj1 bus$3)) same (bundl$3 or group$1 or together or package$1) same ((data adj1 flow adj1 processor$1) or (gate adj1 array$1))	10	L4
JPAB	(bus$3 or (sub adj1 bus$3)) same (bundl$3 or group$1 or together or package$1) same ((data adj1 flow adj1 processor$1) or (gate adj1 array$1))	8	L3
USPT	(bus$3 or (sub adj1 bus$3)) same (bundl$3 or group$1 or together or package$1) same ((data adj1 flow adj1 processor$1) or (gate adj1 array$1))	226	L2
USPT	(bus$3 or (sub adj1 bus$3)) same (bundl$3 or group$1 or together or package$1) same ((data adj1 flow adj1 processor$1) or (programmable adj1 gate adj1 array$1))	61	L1

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Search Results -

Terms	Documents
(bus$3 or (sub adj1 bus$3)) same (bundl$3 or group$1 or together or package$1) same ((data adj1 flow adj1 processor$1) or (gate adj1 array$1))	11

Database:
- US Patents Full-Text Database
- US Pre-Grant Publication Full-Text Database
- JPO Abstracts Database
- EPO Abstracts Database
- Derwent World Patents Index
- IBM Technical Disclosure Bulletins

Refine Search: `(bus$3 or (sub adj1 bus$3)) same (bundl$3 or group$1 or together or package$1) same ((data adj1 flow adj1` Clear

Search History

Today's Date: 4/20/2001

DB Name	Query	Hit Count	Set Name
TDBD	(bus$3 or (sub adj1 bus$3)) same (bundl$3 or group$1 or together or package$1) same ((data adj1 flow adj1 processor$1) or (gate adj1 array$1))	11	L6
DWPI	(bus$3 or (sub adj1 bus$3)) same (bundl$3 or group$1 or together or package$1) same ((data adj1 flow adj1 processor$1) or (gate adj1 array$1))	8	L5
EPAB	(bus$3 or (sub adj1 bus$3)) same (bundl$3 or group$1 or together or package$1) same ((data adj1 flow adj1 processor$1) or (gate adj1 array$1))	10	L4
JPAB	(bus$3 or (sub adj1 bus$3)) same (bundl$3 or group$1 or together or package$1) same ((data adj1 flow adj1 processor$1) or (gate adj1 array$1))	8	L3
USPT	(bus$3 or (sub adj1 bus$3)) same (bundl$3 or group$1 or together or package$1) same ((data adj1 flow adj1 processor$1) or (gate adj1 array$1))	226	L2
USPT	(bus$3 or (sub adj1 bus$3)) same (bundl$3 or group$1 or together or package$1) same ((data adj1 flow adj1 processor$1) or (programmable adj1 gate adj1 array$1))	61	L1

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Search Results -

Terms	Documents
(710/100)!.CCLS. or 710/101.ccls. or 710/8.ccls. or 710/72.ccls. or 710/126.ccls. or 712/11.ccls. or 712/14.ccls. or 712/18.ccls. or 716/16.ccls. or 716/17.ccls. or 326/38.ccls. or 326/39.ccls. or 326/41.ccls. or 439/68.ccls.	4184

Database: US Patents Full-Text Database
US Pre-Grant Publication Full-Text Database
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Derwent World Patents Index
IBM Technical Disclosure Bulletins

Refine Search: (710/100)!.CCLS. or 710/101.ccls. or 710/8.ccls. or 710/72.ccls. or 710/126.ccls. or 712/11.ccls. or

Clear

Search History

Today's Date: 4/20/2001

DB Name	Query	Hit Count	Set Name
USPT	(710/100)!.CCLS. or 710/101.ccls. or 710/8.ccls. or 710/72.ccls. or 710/126.ccls. or 712/11.ccls. or 712/14.ccls. or 712/18.ccls. or 716/16.ccls. or 716/17.ccls. or 326/38.ccls. or 326/39.ccls. or 326/41.ccls. or 439/68.ccls.	4184	L1

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Search Results -

Terms	Documents
l1 and l2	29

Database:
- US Patents Full-Text Database
- US Pre-Grant Publication Full-Text Database
- JPO Abstracts Database
- EPO Abstracts Database
- Derwent World Patents Index
- IBM Technical Disclosure Bulletins

Refine Search: `l1 and l2` Clear

Search History

Today's Date: 4/20/2001

DB Name	Query	Hit Count	Set Name
USPT	l1 and l2	29	L3
USPT	(bus$3 or (sub adj1 bus$3)) same (bundl$4 or group$1 or together or package$1) same ((data adj1 flow adj1 processor$1) or (gate adj1 array$1))	226	L2
USPT	(710/100)!.CCLS. or 710/101.ccls. or 710/8.ccls. or 710/72.ccls. or 710/126.ccls. or 712/11.ccls. or 712/14.ccls. or 712/18.ccls. or 716/16.ccls. or 716/17.ccls. or 326/38.ccls. or 326/39.ccls. or 326/41.ccls. or 439/68.ccls.	4184	L1

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Results are shown **25** to a page, sorted by **publication year** in **descending** order.

You may refine your search by editing the current search expression or entering a new one the text box.

Then click **Search Again**.

((bus*)and ((bundl* or group*))) and(processor?) an Search Again

Results:
Journal or Magazine = **JNL** Conference = **CNF** Standard = **STD**

1 **Parallel Dispatch Queue: a queue-based programming abstraction to parallelize fine-gra communication protocols**
Falsafi, B.; Wood, D.A.
High-Performance Computer Architecture, 1999. Proceedings. Fifth International Symposium On
Page(s): 182 -192

[Abstract] [PDF Full-Text] **CNF**

2 **Proceedings of the Thirtieth Hawaii International Conference on System Sciences**
System Sciences, 1997, Proceedings of the Thirtieth Hwaii International Conference on , Volume:
[Abstract] [PDF Full-Text] **CNF**

3 **Datapath synthesis using onchip multiport memories**
Ahmad, I.; Chen, C.Y.R.
Computers and Digital Techniques, IEE Proceedings E [see also Computers and DigitalTechnique Proceedings-] , Volume: 140 Issue: 4 , July 1993
Page(s): 227 -232

[Abstract] [PDF Full-Text] **JNL**

4 **Proceedings of the Twenty-Fourth Annual Hawaii International Conference on System Sc No.91TH0350-9)**
System Sciences, 1991. Proceedings of the Twenty-Fourth Annual Hawaii International Conference
Volume: i , 1991
[Abstract] [PDF Full-Text] **CNF**

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Generate Collection

L4: Entry 5 of 10 File: EPAB Aug 8, 1995

DOCUMENT-IDENTIFIER: US 5440453 A
TITLE: Extended architecture for FPGA

FPAR:
The invention provides a packaging technique implementing an electronic circuit, comprising several individually packaged sub-circuits, on a circuit board within the footprint of a single package. The embodiment of the present invention is particularly advantageous when implementing application specific integrated circuits (ASICs) or field programmable gate arrays (FPGAs). Selected pins of an upper package are electrically coupled to corresponding pins of the next lower adjacent package such that the pins of the uppermost package can be coupled to the pins of the lowermost package and correspondingly to the signal leads and power bus conductors of the printed circuit board. Portions of selected pins may be removed from one or more packages prior to forming the stacked structure to electrically isolate corresponding pins of upper packages from the pins of lower packages. A template is provided that permits rapid identification of pins to be removed before the packages are configured in the stack. Careful partitioning of the electrical circuit permits a limited number of standard bonding patterns to be combined in a large variety of configurations by rotating packages relative to adjacent packages in the stack. Each package is also provided with additional pins that may be used for vertical routing in a manner that couples non-adjacent packages without coupling to intervening packages. Heat sinks and heat pipes are attachable to the stack to increase thermal dissipation.

WEST

Generate Collection

L3: Entry 5 of 8 File: JPAB Dec 19, 1990

DOCUMENT-IDENTIFIER: JP 02305472 A
TITLE: GATE ARRAY WITH BUILT-IN CPU AND MANUFACTURE THEREOF

FPAR:
PURPOSE: To enable a gate array to be easily designed and to be easily predicted in specification and performance of product before design by a method wherein a wiring pattern is provided to connect the intermediate point of a bus line with the signal terminal of a central processing unit core and the signal terminal of one of cell groups respectively.

WEST

Generate Collection

L3: Entry 7 of 8 File: JPAB Feb 3, 1989

DOCUMENT-IDENTIFIER: JP 01033635 A
TITLE: DATA FLOW PROCESSOR

FPAR:
CONSTITUTION: A link table 11, an operand fetch table 12, a data memory 13, a function table 14, a buffer queue 15, and a processing unit 16 are successively connected together in a ring form via a pipeline type bus. The tokens are transferred along said internal ring bus synchronously with the pipeline clock of a data flow processor 1. When the convolution is carried out with N pieces of data, it is possible to fetch a coefficient w(i) via the table 14 by means of a group identifier of the group tokens. Thus it is not required to make a token train produced by a token producing part 20 make two rounds of the ring bus for fetching N pieces of data and the coefficient w(i). Thus the convolution processing is performed at high speed.

WEST

Generate Collection

L7: Entry 1 of 15 File: USPT Apr 3, 2001

US-PAT-NO: 6211697
DOCUMENT-IDENTIFIER: US 6211697 B1

TITLE: Integrated circuit that includes a field-programmable gate array and a hard gate array having the same underlying structure

DATE-ISSUED: April 3, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Lien; Jung-Cheun	San Jose	CA	N/A	N/A
Feng; Sheng	Cupertino	CA	N/A	N/A
Sun; Chung-yuan	San Jose	CA	N/A	N/A
Huang; Eddy Chieh	San Jose	CA	N/A	N/A

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Actel	Sunnyvale	CA	N/A	N/A	02

APPL-NO: 9/ 318198
DATE FILED: May 25, 1999

INT-CL: [7] H03K 7/38, H03K 19/177
US-CL-ISSUED: 326/41; 326/39
US-CL-CURRENT: 326/41; 326/39
FIELD-OF-SEARCH: 326/38, 326/39, 326/40, 326/41

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	4908528	March 1990	Huang	307/443
☐	5805496	September 1998	Batson et al.	365/154
☐	5809281	September 1998	Steele et al.	395/497.01
☐	5818750	October 1998	Manning	365/154
☐	5825202	October 1998	Tavana et al.	326/39
☐	5841295	November 1998	Kaviani	326/39
☐	6020755	February 2000	Andrews et al.	326/39
☐	6031391	February 2000	Couts-Martin et al.	326/38

ART-UNIT: 289
PRIMARY-EXAMINER: Mai; Son

ATTY-AGENT-FIRM: McCutchen, Doyle, Brown & Enersen, LLP

ABSTRACT:

An integrated circuit (IC) includes both a field-programmable gate array (FPGA) and a hard array (HA). The FPGA includes a first set of functional groups that each include an underlying logic structure and memory cells for programming the underlying logic structure, a first set of routing buses, and a first set of routing interconnect areas that provide interconnections between the first set of functional groups and the first set of routing buses. The first set of routing interconnect areas includes transistors and memory cells for programming the interconnections. The HA includes a second set of functional groups that is equal in number to the first set of functional groups and that are arranged like the first set of functional groups. Each functional group in the second set of functional groups includes an underlying logic structure that is like the underlying logic structure of the first set of functional groups but which does not include memory cells for programming the underlying logic structure. The HA also includes a second set of routing buses that are arranged like the first set of routing buses and a second set of routing interconnect areas that are arranged like the first set of routing interconnect areas but which do not include transistors and memory cells for programming interconnections.

17 Claims, 21 Drawing figures

WEST

Generate Collection

L7: Entry 10 of 15 File: USPT Mar 18, 1997

US-PAT-NO: 5613135
DOCUMENT-IDENTIFIER: US 5613135 A

TITLE: Portable computer having dedicated register group and peripheral controller bus between system bus and peripheral controller

DATE-ISSUED: March 18, 1997

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Sakai; Makoto	Tokyo	N/A	N/A	JPX
Dewa; Koichi	Tokyo	N/A	N/A	JPX
Tsukada; Hiroyuki	Tokyo	N/A	N/A	JPX
Uehara; Keiichi	Tokyo	N/A	N/A	JPX
Mamata; Tohru	Tokyo	N/A	N/A	JPX
Nishino; Yasuhiro	Tokyo	N/A	N/A	JPX
Oda; Hiroyuki	Tokyo	N/A	N/A	JPX

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Kabushiki Kaisha Toshiba	Kanagawa-ken	N/A	N/A	JPX	03

APPL-NO: 8/ 106724
DATE FILED: August 16, 1993

FOREIGN-APPL-PRIORITY-DATA:

COUNTRY	APPL-NO	APPL-DATE
JP	4-248327	September 17, 1992
JP	4-248328	September 17, 1992
JP	4-248356	September 17, 1992
JP	4-272471	September 17, 1992
JP	4-272479	September 17, 1992
JP	4-250165	September 18, 1992
JP	4-255000	September 24, 1992
JP	4-255001	September 24, 1992
JP	4-255004	September 24, 1992

INT-CL: [6] G06F 3/00
US-CL-ISSUED: 395/800; 395/887, 364/234, 364/234.4, 364/DIG.1, 364/928, 364/928.6, 364/DIG.2
US-CL-CURRENT: 710/62; 710/67, 712/43
FIELD-OF-SEARCH: 395/800, 395/275, 395/887, 364/DIG.1, 364/DIG.2, 364/234, 364/234.4, 364/928, 364/928.6

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected | Search ALL

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	4470038	September 1984	Amano et al.	340/365
☐	4621319	November 1986	Braun et al.	364/200
☐	4739310	April 1988	Yamamoto	340/365
☐	5121472	June 1992	Danish et al.	395/275
☐	5138305	August 1992	Tomiyasu	340/717
☐	5241646	August 1993	Arai	395/500
☐	5291585	March 1994	Sato et al.	395/500
☐	5333273	July 1994	Raasch et al.	395/275
☐	5341316	August 1994	Nishigaki	364/709.12
☐	5345392	September 1994	Mito et al.	364/483
☐	5369771	November 1994	Gettel	395/750
☐	5423045	June 1995	Kannan et al.	395/750
☐	5485614	January 1996	Kocis et al.	361/680

FOREIGN PATENT DOCUMENTS

FOREIGN-PAT-NO	PUBN-DATE	COUNTRY	US-CL
0201020	December 1986	EPX	
0358423	March 1990	EPX	

OTHER PUBLICATIONS

Interrupt Protocol for Interconnected Microprocessos, Burmester & Jaschinski, IBM Technical Disclosure Bulletin, vol. 21, No. 2, Jul. 1978, New York, USA, pp. 786-787.

ART-UNIT: 238
PRIMARY-EXAMINER: Black; Thomas G.
ASSISTANT-EXAMINER: Darbe; Valerie
ATTY-AGENT-FIRM: Limbach & Limbach LLP

ABSTRACT:

Dedicated registers are arranged in a status LCD control gate array connected to a system bus, and the dedicated registers or register group and a keyboard controller are connected through a keyboard interface bus. The keyboard controller has two ports for communicating with a CPU. The keyboard controller transfers existing commands released to an application program or the like and transmits normal key data through the system bus. The keyboard controller transmits hot key data and transfers a command for realizing any other special function through the keyboard interface bus and the dedicated registers.

3 Claims, 78 Drawing figures

WEST

Generate Collection

L7: Entry 12 of 15 File: USPT Aug 8, 1995

US-PAT-NO: 5440453
DOCUMENT-IDENTIFIER: US 5440453 A

TITLE: Extended architecture for FPGA

DATE-ISSUED: August 8, 1995

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Cooke; Laurance H.	San Jose	CA	N/A	N/A
Penry; Matthew D.	Modesto	CA	N/A	N/A

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Crosspoint Solutions, Inc.	Santa Clara	CA	N/A	N/A	02

APPL-NO: 8/ 152267
DATE FILED: November 12, 1993

PARENT-CASE:
This is a Continuation of application Ser. No. 07/809,745, filed Dec. 18, 1991, now abandoned.

INT-CL: [6] H01R 23/68
US-CL-ISSUED: 361/790; 361/744, 361/791, 361/792, 257/697, 439/69, 174/262
US-CL-CURRENT: 361/790; 174/262, 257/697, 361/744, 361/791, 361/792, 439/69
FIELD-OF-SEARCH: 361/744, 361/748, 361/767, 361/772, 361/776, 361/792, 361/791, 361/790, 361/794, 361/799, 257/686, 257/697, 439/45, 439/69, 439/74, 439/75, 174/52.4, 174/261, 174/262

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	3676748	July 1972	Kobayashi et al.	N/A
☐	3718750	February 1973	Sayers et al.	N/A
☐	3764856	October 1973	Martin	317/100
☐	3777221	December 1973	Tatusko et al.	N/A
☐	3999105	December 1976	Archey et al.	N/A
☐	4103321	July 1978	Gansert et al.	N/A
☐	4137559	January 1979	Reuting	N/A
☐	4338652	July 1982	Romanczuk et al.	N/A
☐	4514784	April 1985	Williams et al.	N/A
☐	4620632	November 1986	Alemanni	N/A
☐	4630172	December 1986	Stenerson et al.	N/A
☐	4654694	March 1987	Val	N/A
☐	4729061	March 1988	Brown	N/A
☐	4920454	April 1990	Stopper et al.	N/A
☐	4953060	August 1990	Lauffer et al.	361/388
☐	5128831	July 1992	Fox, III et al.	361/396

ART-UNIT: 213
PRIMARY-EXAMINER: Picard; Leo P.
ASSISTANT-EXAMINER: Whang; Young
ATTY-AGENT-FIRM: Townsend and Townsend Khourie and Crew

ABSTRACT:

The invention provides a packaging technique implementing an electronic circuit, comprising several individually packaged sub-circuits, on a circuit board within the footprint of a single package. The embodiment of the present invention is particularly advantageous when implementing application specific integrated circuits (ASICs) or field programmable gate arrays (FPGAs). Selected pins of an upper package are electrically coupled to corresponding pins of the next lower adjacent package such that the pins of the uppermost package can be coupled to the pins of the lowermost package and correspondingly to the signal leads and power bus conductors of the printed circuit board. Portions of selected pins may be removed from one or more packages prior to forming the stacked structure to electrically isolate corresponding pins of upper packages from the pins of lower packages. A template is provided that permits rapid identification of pins to be removed before the packages are configured in the stack.

Careful partitioning of the electrical circuit permits a limited number of standard bonding patterns to be combined in a large variety of configurations by rotating packages relative to adjacent packages in the stack. Each package is also provided with additional pins that may be used for vertical routing in a manner that couples non-adjacent packages without coupling to intervening packages. Heat sinks and heat pipes are attachable to the stack to increase thermal dissipation.

32 Claims, 10 Drawing figures

WEST

End of Result Set

Generate Collection

L8: Entry 1 of 1 File: USPT Sep 12, 2000

US-PAT-NO: 6119181
DOCUMENT-IDENTIFIER: US 6119181 A

TITLE: I/O and memory bus system for DFPs and units with two- or multi-dimensional programmable cell architectures

DATE-ISSUED: September 12, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Vorbach; Martin	Karlsruhe	N/A	N/A	DEX
Munch; Robert	Karlsruhe	N/A	N/A	DEX

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
PACT GmbH	Munich	N/A	N/A	DEX	03

APPL-NO: 8/ 947254
DATE FILED: October 8, 1997

FOREIGN-APPL-PRIORITY-DATA:

COUNTRY	APPL-NO	APPL-DATE
DE	196 54 595	December 20, 1996

INT-CL: [7] G06F 13/40, G06F 15/80
US-CL-ISSUED: 710/100; 710/110, 710/129, 712/11
US-CL-CURRENT: 710/100; 710/110, 710/129, 712/11
FIELD-OF-SEARCH: 395/280, 395/309, 395/800.11, 395/80.25, 395/800.29, 395/377, 326/38, 326/39, 326/41, 364/489, 370/419, 710/100, 710/129, 710/110, 712/11, 712/14, 712/18, 712/25, 712/29, 712/31, 711/100

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	Re34363	August 1993	Freeman	326/38
☐	4706216	November 1987	Carter	365/94
☐	4739474	April 1988	Holsztynski et al.	395/800.14
☐	4761755	August 1988	Ardini et al.	364/749
☐	4811214	March 1989	Nosenchuck et al.	395/800.11
☐	4852048	July 1989	Morton	712/11
☐	4870302	September 1989	Freeman	326/41

4901268	February 1990	Judd	364/748.19
4967340	October 1990	Dawes	395/800.19
5014193	May 1991	Garner et al.	395/830
5015884	May 1991	Agrawal et al.	326/39
5021947	June 1991	Campbell et al.	395/800.25
5023775	June 1991	Poret	326/40
5081375	January 1992	Pickett et al.	326/41
5109503	April 1992	Cruickshank et al.	395/500
5113498	May 1992	Evan et al.	395/828
5123109	June 1992	Hillis	395/800.22
5125801	June 1992	Nabity et al.	417/44.1
5128559	July 1992	Steele	326/38
5142469	August 1992	Weisenborn	364/146
5204935	April 1993	Mihara et al.	706/4
5208491	May 1993	Ebeling et al.	326/41
5226122	July 1993	Thayer et al.	395/500
5233539	August 1993	Agrawal et al.	364/489
5247689	September 1993	Ewert	395/311
5287472	February 1994	Horst	365/189.08
5301344	April 1994	Kolchinsky	395/800.32
5303172	April 1994	Magar et al.	364/726.04
5336950	August 1994	Popli et al.	326/39
5361373	November 1994	Gilson	395/800.01
5418952	May 1995	Morley et al.	395/800.14
5421019	May 1995	Holsztynski et al.	395/800.14
5422823	June 1995	Agrawal et al.	364/489
5426378	June 1995	Ong	326/39
5430687	July 1995	Hung et al.	365/230.08
5440245	August 1995	Galbraith et al.	326/38
5442790	August 1995	Nosenchuck	395/707
5444394	August 1995	Watson et al.	326/45
5448186	September 1995	Kawata	326/41
5455525	October 1995	Ho et al.	326/41
5457644	October 1995	McCollum	364/716.01
5473266	December 1995	Ahanin et al.	326/41
5473267	December 1995	Stansfield	326/41
5475583	December 1995	Bock et al.	364/141
5475803	December 1995	Stearns et al.	345/436

☐	5483620	January 1996	Pechanek et al.	706/41
☐	5485103	January 1996	Pedersen et al.	326/41
☐	5485104	January 1996	Agrawal et al.	326/38
☐	5489857	February 1996	Agrawal et al.	326/41
☐	5491353	February 1996	Kean	257/208
☐	5493239	February 1996	Zlotnick	326/38
☐	5497498	March 1996	Taylor	395/284
☐	5506998	April 1996	Kato et al.	395/800.29
☐	5510730	April 1996	El Gamal et al.	326/41
☐	5511173	April 1996	Yamaura et al.	395/598
☐	5513366	April 1996	Agarwal et al.	395/800.22
☐	5521837	May 1996	Frankle et al.	364/491
☐	5522083	May 1996	Gove et al.	395/800.22
☐	5532693	July 1996	Winters et al.	341/51
☐	5532957	July 1996	Malhi	365/154
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☐	5537057	July 1996	Leong et al.	326/41
☐	5537601	July 1996	Kimura et al.	395/800.35
☐	5541530	July 1996	Cliff et al.	326/41
☐	5544336	August 1996	Kato et al.	395/311
☐	5548773	August 1996	Kemney et al.	395/800.11
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☐	5559450	September 1996	Ngai et al.	326/40
☐	5561738	October 1996	Kinerk et al.	706/4
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☐	5583450	December 1996	Trimberger et al.	326/41
☐	5586044	December 1996	Agrawal et al.	364/489
☐	5587921	December 1996	Agrawal et al.	364/489
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0 221 360	May 1987	EPX	
0428327A1	May 1991	EPX	
748 051 A2	December 1991	EPX	
0539595A1	May 1993	EPX	
0 678 985	October 1995	EPX	
0 726 532	August 1996	EPX	
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Maxfield C. "Logic that Mutates While-U-Wait" EDN (Bur. Ed) (USA), EDN (European Edition), Nov. 7, 1996, Cahners Publishing, USA.

ART-UNIT: 271
PRIMARY-EXAMINER: Ray; Gopal C.
ATTY-AGENT-FIRM: Kenyon & Kenyon

ABSTRACT:

A uniform bus system is provided which operates without any special consideration by a programmer. Memories and peripheral may be connected to this bus system without any special measures. Likewise, units may be cascaded with the help of the bus system. The bus system combines a number of internal lines, and leads them as a bundle to terminals. The bus system control is predefined and does not require any influence by the programmer. Any number of memories, peripherals or other units can be connected to the bus system.

35 Claims, 20 Drawing figures

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L1: Entry 1 of 1 File: USPT Jun 22, 1999

US-PAT-NO: 5915123
DOCUMENT-IDENTIFIER: US 5915123 A

TITLE: Method and apparatus for controlling configuration memory contexts of processing elements in a network of multiple context processing elements

DATE-ISSUED: June 22, 1999

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Mirsky; Ethan	Mountain View	CA	N/A	N/A
French; Robert	Sunnyvale	CA	N/A	N/A
Eslick; Ian	Mountain View	CA	N/A	N/A

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Silicon Spice	Mountain View	CA	N/A	N/A	02

APPL-NO: 8/ 962141
DATE FILED: October 31, 1997

INT-CL: [6] G06F 15/177, H03K 19/177
US-CL-ISSUED: 395/800.16; 326/37, 326/38, 326/39, 395/653
US-CL-CURRENT: 712/16; 326/37, 326/38, 326/39
FIELD-OF-SEARCH: 326/38, 326/39, 326/37, 395/651, 395/653, 395/800.14, 395/800.15, 395/800.16

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	4597041	June 1986	Guyer et al.	395/598
☐	4748585	May 1988	Chiarulli et al.	395/800.15
☐	4754412	June 1988	Deering	364/736.05
☐	4858113	August 1989	Saccardi	395/312
☐	4870302	September 1989	Freeman	326/41
☐	5020059	May 1991	Gorin et al.	395/182.01
☐	5233539	August 1993	Agrawal et al.	364/489
☐	5301340	April 1994	Cook	395/800.24
☐	5336950	August 1994	Popli et al.	326/39
☐	5426378	June 1995	Ong	326/39
☐	5457408	October 1995	Leung	326/38
☐	5469003	November 1995	Kean	326/39
☐	5684980	November 1997	Casselman	395/500
☐	5742180	April 1998	Detton et al.	326/80
☐	5754818	May 1998	Mohamed	711/207
☐	5765209	June 1998	Yetter	711/207
☐	5778439	July 1998	Trinberger et al.	711/153

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Baker; "Programming Silicon"; Aug. 28, 1995; Electronic Engineering Times; p. 73.
Brown; "Smart Compilers Puncture Code Bloat"; Oct. 9, 1995; Electronic Engineering Times; pp. 38 and 42.
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Wang, et al.; "Distributed Instruction Set Computer"; Proceedings of the 1988 International Conference on Parallel Processing; Aug. 15-19, 1988; pp. 426-429.

ART-UNIT: 273
PRIMARY-EXAMINER: Kim; Kenneth S.
ATTY-AGENT-FIRM: Blakely, Sokoloff, Taylor & Zafman

ABSTRACT:

A method and apparatus for providing local control of processing elements in a network of multiple context processing element are provided. A multiple context processing element is configured to store a number of configuration memory contexts. This multiple context processing element maintains data of a current configuration. State information is received from at least one other multiple context processing element. At least one configuration control signal is generated in response to the state information and the data of a current configuration. One of multiple configuration memory contexts is selected in response to the configuration control signal, the selected configuration memory context controlling the multiple context processing element. Each multiple context processing element in the networked array of multiple context processing elements has an assigned physical and virtual identification. Data is transmitted to at least one of the multiple context processing elements of the array, the data comprising control data, configuration data, an address mask, and a destination identification. The transmitted address mask is applied to either the physical or virtual identification and to a destination identification. The masked physical or virtual identification is compared to the masked destination identification. When the masked physical or virtual identification of a multiple context processing element matches the masked destination identification, at least one of the number of multiple context processing elements are manipulated in response to the transmitted data. Manipulation comprises selecting one of a number of configuration memory contexts to control the functioning of the multiple context processing element.

26 Claims, 23 Drawing figures

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Database:
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- EPO Abstracts Database
- Derwent World Patents Index
- IBM Technical Disclosure Bulletins

Refine Search: 4489857.pn. or 4591979.pn. or 5043978.pn. or 5115510.pn. or 5208491.pn. or 5440245.pn. or

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USPT	5892961.pn.	1	L2
USPT	5915123.pn.	1	L1

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Search Results - Record(s) 1 through 10 of 13 returned.

☐ 1. Document ID: US 5713037 A

L3: Entry 1 of 13 File: USPT Jan 27, 1998

US-PAT-NO: 5713037
DOCUMENT-IDENTIFIER: US 5713037 A
TITLE: Slide bus communication functions for SIMD/MIMD array processor

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

☐ 2. Document ID: US 5655124 A

L3: Entry 2 of 13 File: USPT Aug 5, 1997

US-PAT-NO: 5655124
DOCUMENT-IDENTIFIER: US 5655124 A
TITLE: Selective power-down for high performance CPU/system

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

☐ 3. Document ID: US 5652894 A

L3: Entry 3 of 13 File: USPT Jul 29, 1997

US-PAT-NO: 5652894
DOCUMENT-IDENTIFIER: US 5652894 A
TITLE: Method and apparatus for providing power saving modes to a pipelined processor

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

☐ 4. Document ID: US 5634131 A

L3: Entry 4 of 13 File: USPT May 27, 1997

US-PAT-NO: 5634131
DOCUMENT-IDENTIFIER: US 5634131 A
TITLE: Method and apparatus for independently stopping and restarting functional units

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

☐ 5. Document ID: US 5617547 A

L3: Entry 5 of 13 File: USPT Apr 1, 1997

US-PAT-NO: 5617547
DOCUMENT-IDENTIFIER: US 5617547 A
TITLE: Switch network extension of bus architecture

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

☐ 6. Document ID: US 5596742 A

L3: Entry 6 of 13 File: USPT Jan 21, 1997

US-PAT-NO: 5596742
DOCUMENT-IDENTIFIER: US 5596742 A
TITLE: Virtual interconnections for reconfigurable logic systems

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

☐ 7. Document ID: US 5590348 A

L3: Entry 7 of 13 File: USPT Dec 31, 1996

US-PAT-NO: 5590348
DOCUMENT-IDENTIFIER: US 5590348 A
TITLE: Status predictor for combined shifter-rotate/merge unit

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

☐ 8. Document ID: US 5440245 A

L3: Entry 8 of 13 File: USPT Aug 8, 1995

US-PAT-NO: 5440245
DOCUMENT-IDENTIFIER: US 5440245 A
TITLE: Logic module with configurable combinational and sequential blocks

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

☐ 9. Document ID: US 5208491 A

L3: Entry 9 of 13 File: USPT May 4, 1993

US-PAT-NO: 5208491
DOCUMENT-IDENTIFIER: US 5208491 A
TITLE: Field programmable gate array

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw. Desc | Image

☐ 10. Document ID: US 5115510 A

L3: Entry 10 of 13 File: USPT May 19, 1992

US-PAT-NO: 5115510
DOCUMENT-IDENTIFIER: US 5115510 A
TITLE: Multistage data flow processor with instruction packet, fetch, storage transmission and address generation controlled by destination information

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw. Desc | Image

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4489857.pn. or 4591979.pn. or 5043978.pn. or 5115510.pn. or 5208491.pn. or 5440245.pn. or 5590348.pn. or 5596742.pn. or 5617547.pn. 5634131.pn. or 5652894.pn. or 5655124.pn. or 5713037.pn.	13

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☐ 11. Document ID: US 5043978 A

L3: Entry 11 of 13 File: USPT Aug 27, 1991

US-PAT-NO: 5043978
DOCUMENT-IDENTIFIER: US 5043978 A
TITLE: Circuit arrangement for telecommunications exchanges

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw. Desc | Image

☐ 12. Document ID: US 4591979 A

L3: Entry 12 of 13 File: USPT May 27, 1986

US-PAT-NO: 4591979
DOCUMENT-IDENTIFIER: US 4591979 A
TITLE: Data-flow-type digital processing apparatus

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw. Desc | Image

☐ 13. Document ID: US 4489857 A

L3: Entry 13 of 13 File: USPT Dec 25, 1984

US-PAT-NO: 4489857
DOCUMENT-IDENTIFIER: US 4489857 A
TITLE: Liquid dispenser

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw. Desc | Image

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Database: US Patents Full-Text Database; US Pre-Grant Publication Full-Text Database; JPO Abstracts Database; EPO Abstracts Database; Derwent World Patents Index; IBM Technical Disclosure Bulletins

Refine Search: 5717943.pn. or 5734921.pn. or 5742180.pn. or 5748872.pn. or 5754871.pn. or 5761484.pn. or

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USPT	5717943.pn. or 5734921.pn. or 5742180.pn. or 5748872.pn. or 5754871.pn. or 5761484.pn. or 5778439.pn. or 5801715.pn. or 5828858.pn. or 5838165.pn. or 5867691.pn. or 5892961.pn. or 5915123.pn. or 5927423.pn. or 5936424.pn. or 5956518.pn. or 6014509.pn. or 6052773.pn. or 6054873.pn. or 6108760.pn. or 6122719.pn. or 6127908.pn.	22	L4
USPT	4489857.pn. or 4591979.pn. or 5043978.pn. or 5115510.pn. or 5208491.pn. or 5440245.pn. or 5590348.pn. or 5596742.pn. or 5617547.pn. 5634131.pn. or 5652894.pn. or 5655124.pn. or 5713037.pn.	13	L3
USPT	5892961.pn.	1	L2
USPT	5915123.pn.	1	L1

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Search Results - Record(s) 1 through 10 of 22 returned.

1. Document ID: US 6127908 A

L4: Entry 1 of 22 File: USPT Oct 3, 2000

US-PAT-NO: 6127908
DOCUMENT-IDENTIFIER: US 6127908 A
TITLE: Microelectro-mechanical system actuator device and reconfigurable circuits utilizing same

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

2. Document ID: US 6122719 A

L4: Entry 2 of 22 File: USPT Sep 19, 2000

US-PAT-NO: 6122719
DOCUMENT-IDENTIFIER: US 6122719 A
TITLE: Method and apparatus for retiming in a network of multiple context processing elements

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

3. Document ID: US 6108760 A

L4: Entry 3 of 22 File: USPT Aug 22, 2000

US-PAT-NO: 6108760
DOCUMENT-IDENTIFIER: US 6108760 A
TITLE: Method and apparatus for position independent reconfiguration in a network of multiple context processing elements

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

4. Document ID: US 6054873 A

L4: Entry 4 of 22 File: USPT Apr 25, 2000

US-PAT-NO: 6054873
DOCUMENT-IDENTIFIER: US 6054873 A
TITLE: Interconnect structure between heterogeneous core regions in a programmable array

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

☐ 5. Document ID: US 6052773 A

L4: Entry 5 of 22 File: USPT Apr 18, 2000

US-PAT-NO: 6052773
DOCUMENT-IDENTIFIER: US 6052773 A
TITLE: DPGA-coupled microprocessors

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

☐ 6. Document ID: US 6014509 A

L4: Entry 6 of 22 File: USPT Jan 11, 2000

US-PAT-NO: 6014509
DOCUMENT-IDENTIFIER: US 6014509 A
TITLE: Field programmable gate array having access to orthogonal and diagonal adjacent neighboring cells

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

☐ 7. Document ID: US 5956518 A

L4: Entry 7 of 22 File: USPT Sep 21, 1999

US-PAT-NO: 5956518
DOCUMENT-IDENTIFIER: US 5956518 A
TITLE: Intermediate-grain reconfigurable processing device

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

☐ 8. Document ID: US 5936424 A

L4: Entry 8 of 22 File: USPT Aug 10, 1999

US-PAT-NO: 5936424
DOCUMENT-IDENTIFIER: US 5936424 A
TITLE: High speed bus with tree structure for selecting bus driver

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

☐ 9. Document ID: US 5927423 A

L4: Entry 9 of 22 File: USPT Jul 27, 1999

US-PAT-NO: 5927423
DOCUMENT-IDENTIFIER: US 5927423 A
TITLE: Reconfigurable footprint mechanism for omnidirectional vehicles

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

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☐ 10. Document ID: US 5915123 A

L4: Entry 10 of 22 File: USPT Jun 22, 1999

US-PAT-NO: 5915123
DOCUMENT-IDENTIFIER: US 5915123 A
TITLE: Method and apparatus for controlling configuration memory contexts of processing elements in a network of multiple context processing elements

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

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Terms	Documents
5717943.pn. or 5734921.pn. or 5742180.pn. or 5748872.pn. or 5754871.pn. or 5761484.pn. or 5778439.pn. or 5801715.pn. or 5828858.pn. or 5838165.pn. or 5867691.pn. or 5892961.pn. or 5915123.pn. or 5927423.pn. or 5936424.pn. or 5956518.pn. or 6014509.pn. or 6052773.pn. or 6054873.pn. or 6108760.pn. or 6122719.pn. or 6127908.pn.	22

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☐ 11. Document ID: US 5892961 A

L4: Entry 11 of 22 File: USPT Apr 6, 1999

US-PAT-NO: 5892961
DOCUMENT-IDENTIFIER: US 5892961 A
TITLE: Field programmable gate array having programming instructions in the configuration bitstream

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

☐ 12. Document ID: US 5867691 A

L4: Entry 12 of 22 File: USPT Feb 2, 1999

US-PAT-NO: 5867691
DOCUMENT-IDENTIFIER: US 5867691 A
TITLE: Synchronizing system between function blocks arranged in hierarchical structures and large scale integrated circuit using the same

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

☐ 13. Document ID: US 5838165 A

L4: Entry 13 of 22 File: USPT Nov 17, 1998

US-PAT-NO: 5838165
DOCUMENT-IDENTIFIER: US 5838165 A
TITLE: High performance self modifying on-the-fly alterable logic FPGA, architecture and method

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

☐ 14. Document ID: US 5828858 A

L4: Entry 14 of 22 File: USPT Oct 27, 1998

US-PAT-NO: 5828858
DOCUMENT-IDENTIFIER: US 5828858 A
TITLE: Worm-hole run-time reconfigurable processor field programmable gate array (FPGA)

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

☐ 15. Document ID: US 5801715 A

L4: Entry 15 of 22 File: USPT Sep 1, 1998

US-PAT-NO: 5801715
DOCUMENT-IDENTIFIER: US 5801715 A
TITLE: Massively-parallel processor array with outputs from individual processors directly to an external device without involving other processors or a common physical carrier

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

☐ 16. Document ID: US 5778439 A

L4: Entry 16 of 22 File: USPT Jul 7, 1998

US-PAT-NO: 5778439
DOCUMENT-IDENTIFIER: US 5778439 A
TITLE: Programmable logic device with hierarchical configuration and state storage

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

☐ 17. Document ID: US 5761484 A

L4: Entry 17 of 22 File: USPT Jun 2, 1998

US-PAT-NO: 5761484
DOCUMENT-IDENTIFIER: US 5761484 A
TITLE: Virtual interconnections for reconfigurable logic systems

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

☐ 18. Document ID: US 5754871 A

L4: Entry 18 of 22 File: USPT May 19, 1998

US-PAT-NO: 5754871
DOCUMENT-IDENTIFIER: US 5754871 A
TITLE: Parallel processing system having asynchronous SIMD processing

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

☐ 19. Document ID: US 5748872 A

L4: Entry 19 of 22 File: USPT May 5, 1998

US-PAT-NO: 5748872
DOCUMENT-IDENTIFIER: US 5748872 A
TITLE: Direct replacement cell fault tolerant architecture

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

☐ 20. Document ID: US 5742180 A

L4: Entry 20 of 22 File: USPT Apr 21, 1998

US-PAT-NO: 5742180
DOCUMENT-IDENTIFIER: US 5742180 A
TITLE: Dynamically programmable gate array with multiple contexts

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

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5717943.pn. or 5734921.pn. or 5742180.pn. or 5748872.pn. or 5754871.pn. or 5761484.pn. or 5778439.pn. or 5801715.pn. or 5828858.pn. or 5838165.pn. or 5867691.pn. or 5892961.pn. or 5915123.pn. or 5927423.pn. or 5936424.pn. or 5956518.pn. or 6014509.pn. or 6052773.pn. or 6054873.pn. or 6108760.pn. or 6122719.pn. or 6127908.pn.	22

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Search Results - Record(s) 21 through 22 of 22 returned.

☐ 21. Document ID: US 5734921 A

L4: Entry 21 of 22 File: USPT Mar 31, 1998

US-PAT-NO: 5734921
DOCUMENT-IDENTIFIER: US 5734921 A
TITLE: Advanced parallel array processor computer package

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

☐ 22. Document ID: US 5717943 A

L4: Entry 22 of 22 File: USPT Feb 10, 1998

US-PAT-NO: 5717943
DOCUMENT-IDENTIFIER: US 5717943 A
TITLE: Advanced parallel array processor (APAP)

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

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5717943.pn. or 5734921.pn. or 5742180.pn. or 5748872.pn. or 5754871.pn. or 5761484.pn. or 5778439.pn. or 5801715.pn. or 5828858.pn. or 5838165.pn. or 5867691.pn. or 5892961.pn. or 5915123.pn. or 5927423.pn. or 5936424.pn. or 5956518.pn. or 6014509.pn. or 6052773.pn. or 6054873.pn. or 6108760.pn. or 6122719.pn. or 6127908.pn.	22

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